República Bolivariana de Venezuela

Universidad de Carabobo

Facultad de Ingeniería

Escuela de Ingeniería Eléctrica y de Telecomunicaciones

Departamento de Sistemas y Automática

Cátedra de Lógica Digital

**Práctica # 4 – Sesión #02**

**Objetivo: Diseñar e implementar circuitos combinacionales con Multiplexores y Demultiplexores utilizando VHDL y la tarjeta de desarrollo BASYS2**

Sección #05 de Laboratorio

**Integrantes:**

Carlos Hernández

C.I.: 25.829.471

Gianfranco Gasbarri

C.I.: 26.654.860

Fecha de entrega: 19/03/19

**Pre-Laboratorio**

1. **Desarrollo de componente MUX21:** Ver **Anexo 1**
2. **Desarrollo de componente MUX41 mediante árbol de multiplexores 2:1:** Ver **Anexo 2**
3. **Desarrollo de componente DEMUX14:** Ver **Anexo 3**
4. **Desarrollo de componente Codificador3:2:** Ver **Anexo 4**
5. **Problema “Sistema”:** Ver **Anexo 5**

**Laboratorio**

1. **Diseño de alto nivel:** Ver **Anexo 6**

**ANEXOS**

**Anexo 1**

**Anexo 1.1**

**Diagrama de caja negra**

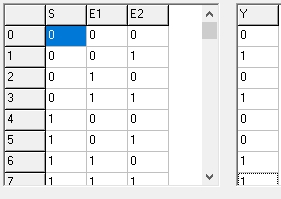
**S**

**MUX 2:1**

**Y**

**Anexo 1.2**

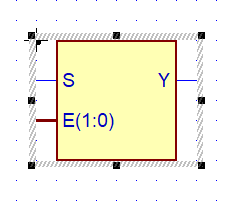
**Tabla de la verdad**





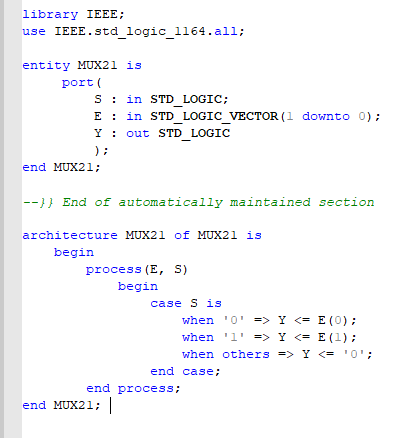
**Anexo 1.3**

**Símbolo**



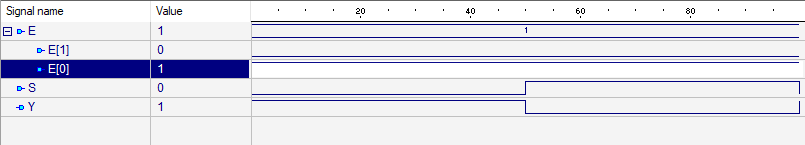
**Anexo 1.4**

**Código VHDL**



**Anexo 1.5**

**Simulación**



**Anexo 2**

**Anexo 2.1**

**Diagrama de caja negra**

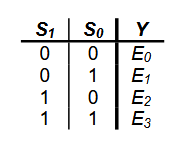
**S**

**MUX 4:1**

**Y**

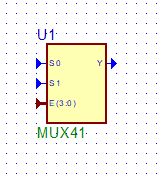
**Anexo 2.2**

**Tabla de la verdad**



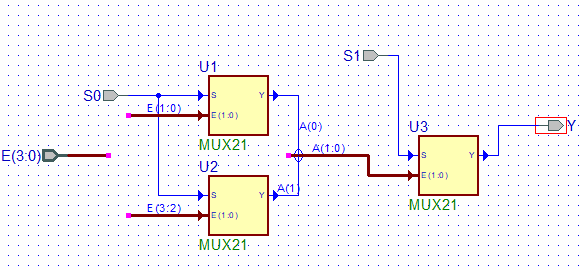
**Anexo 2.3**

**Símbolo**



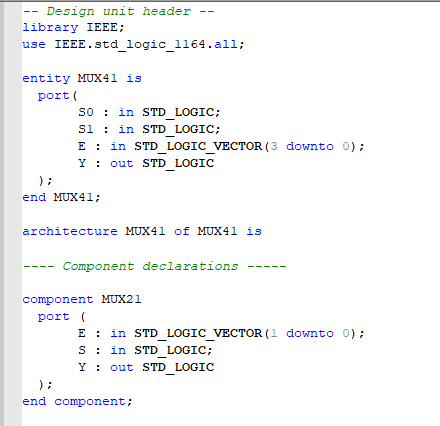
**Anexo 2.4**

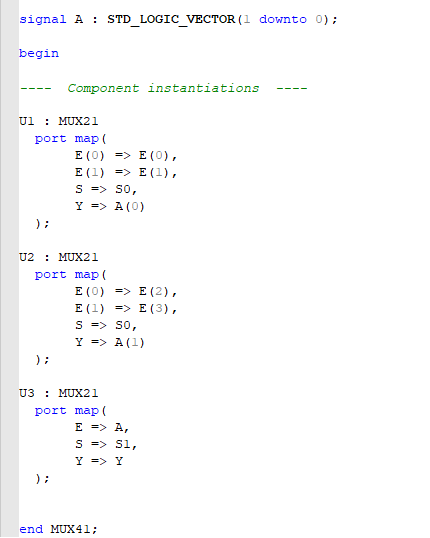
**Diseño**



**Anexo 2.5**

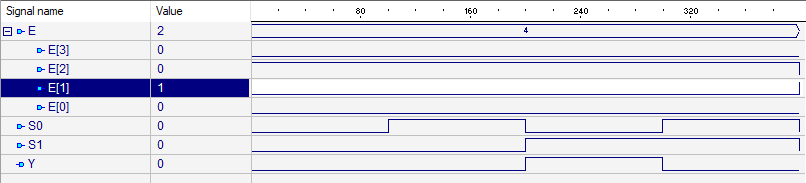
**Código VHDL**





**Anexo 2.6**

**Simulación**



**Anexo 3**

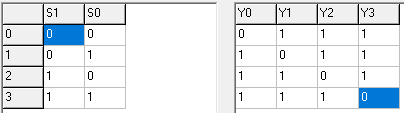
**Anexo 3.1**

**Diagrama de caja negra**

**DEMUX 1:4**

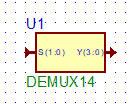
**Anexo 3.2**

**Tabla de la verdad**



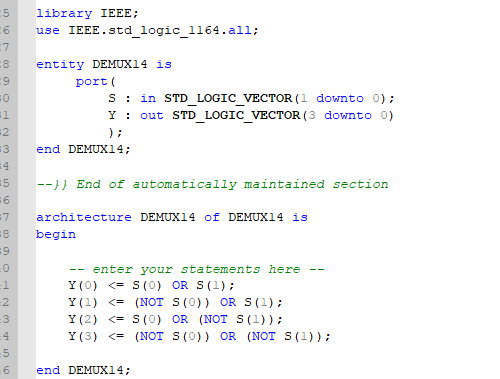
**Anexo 3.3**

**Símbolo**



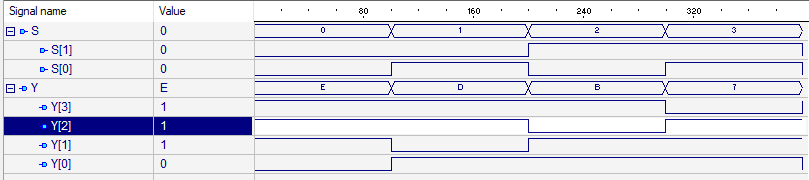
**Anexo 3.4**

**Código VHDL**



**Anexo 3.5**

**Simulación**



**Anexo 4**

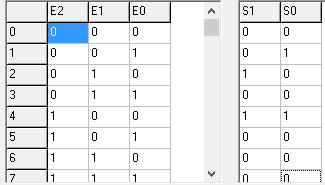
**Anexo 3.1**

**Diagrama de caja negra**

**Codificador3:2**

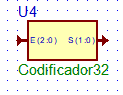
**Anexo 3.2**

**Tabla de la verdad**



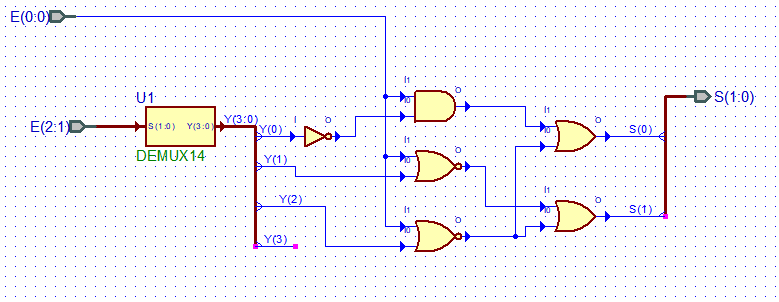
**Anexo 3.3**

**Símbolo**



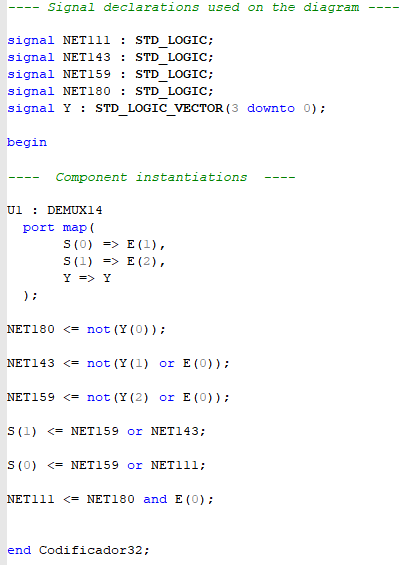
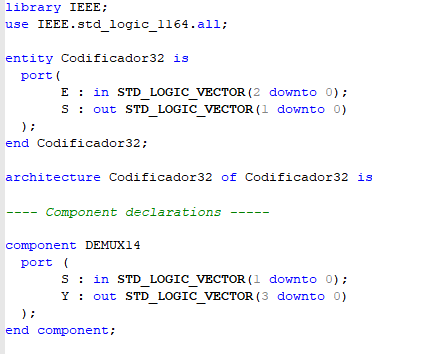
**Anexo 3.4**

**Diseño**



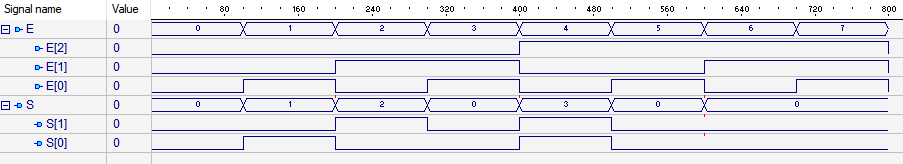
**Anexo 3.5**

**Código VHDL**



**Anexo 3.6**

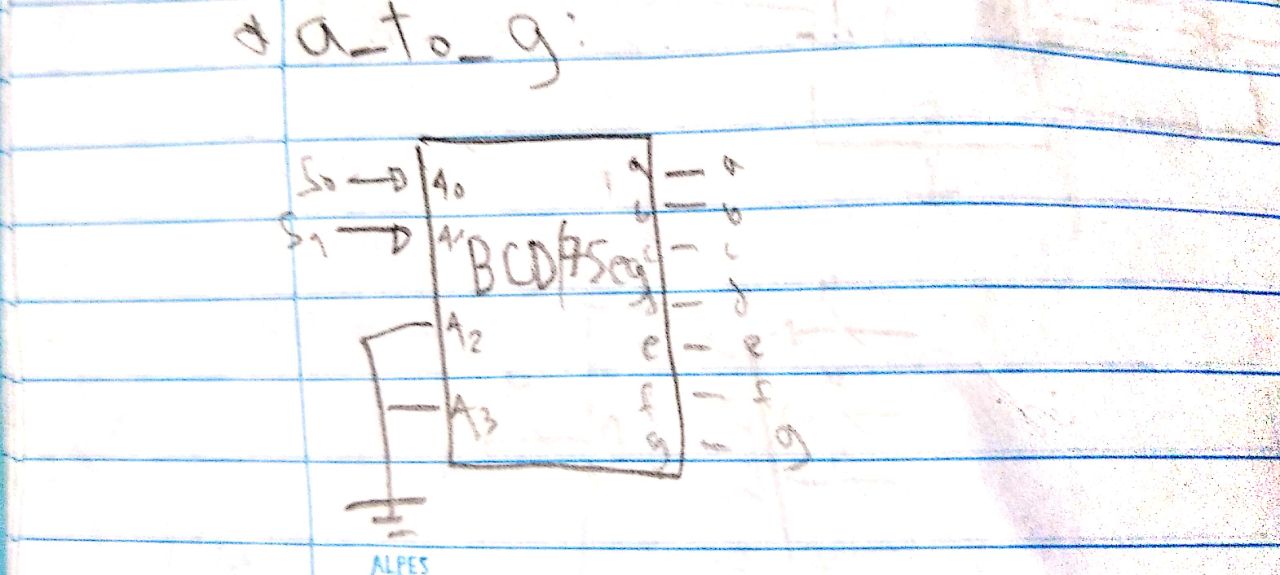
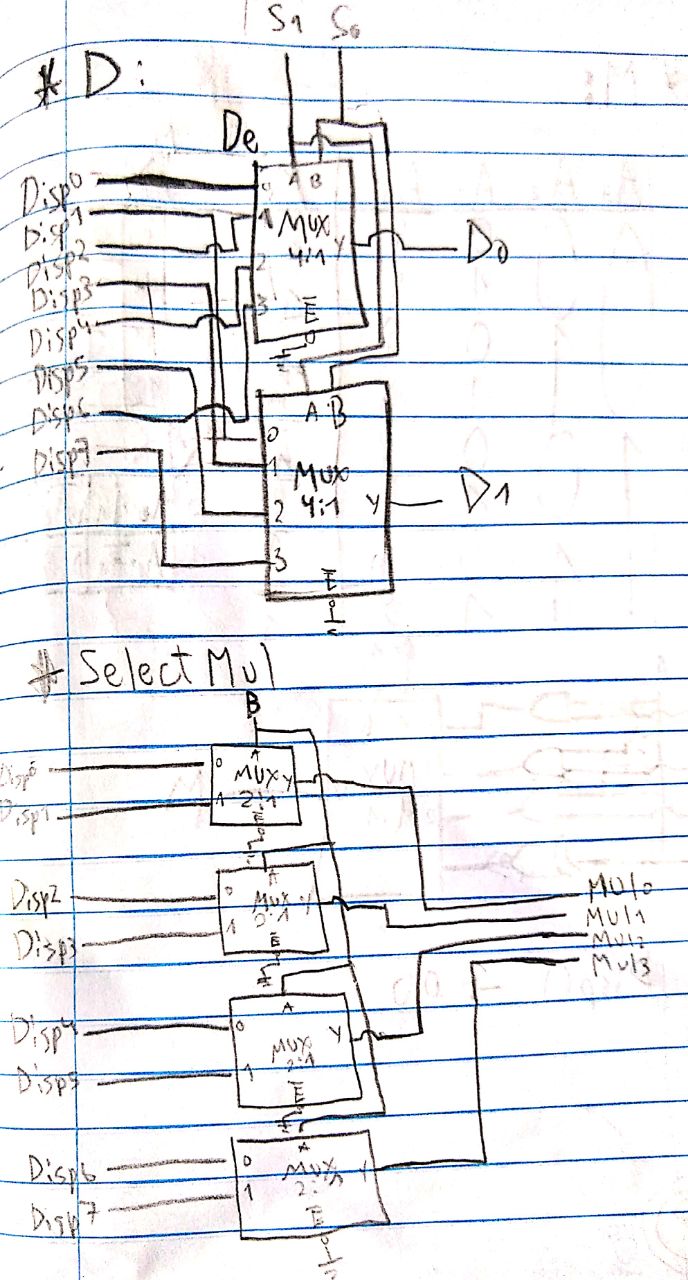
**Simulación**

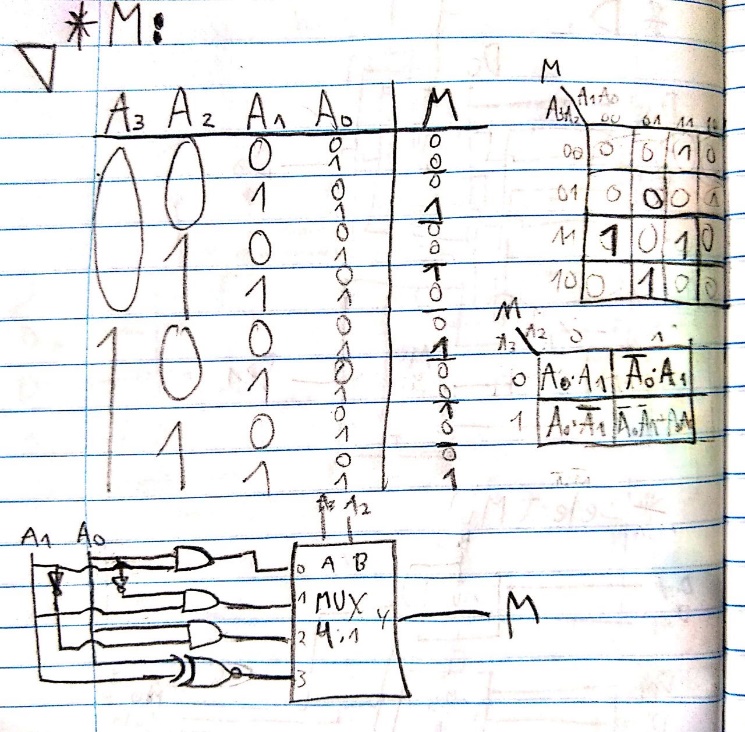


**Anexo 5: Problema “Sistema”**

**Anexo 5.1**

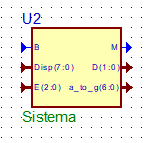
**Análisis**

****

****

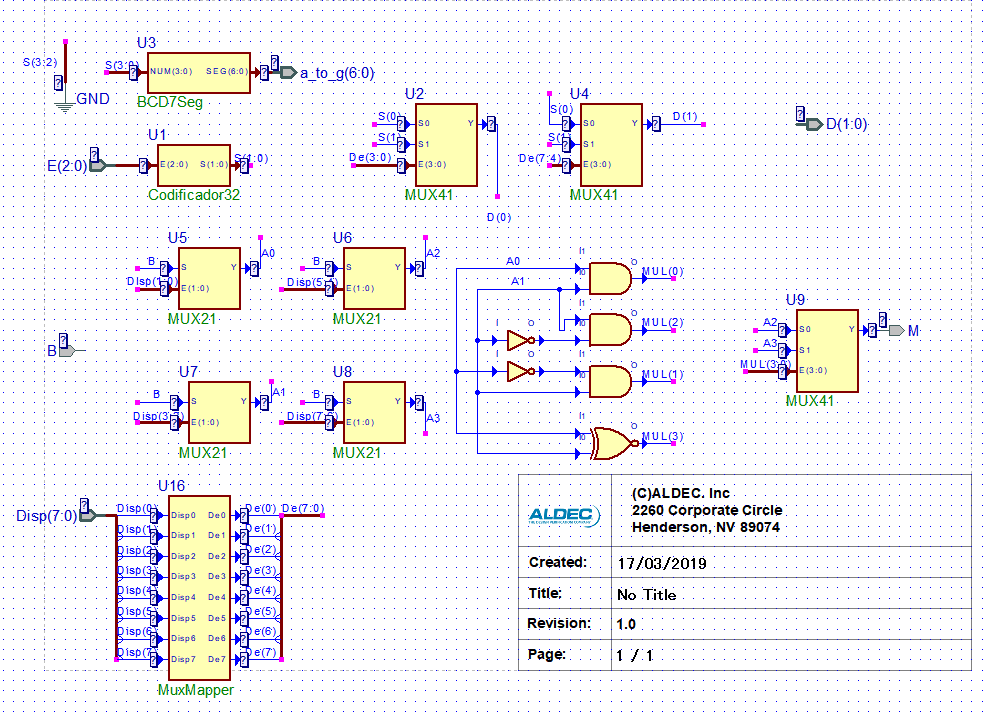
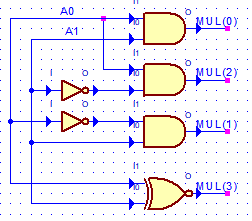
**Anexo 5.2**

**Símbolo**



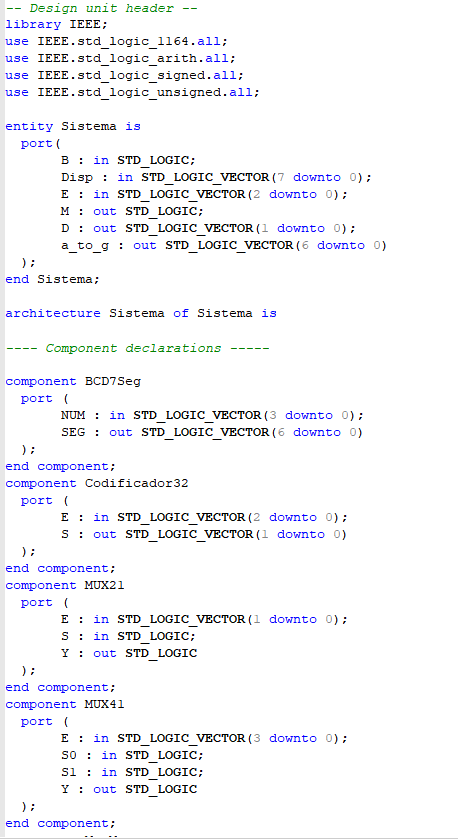
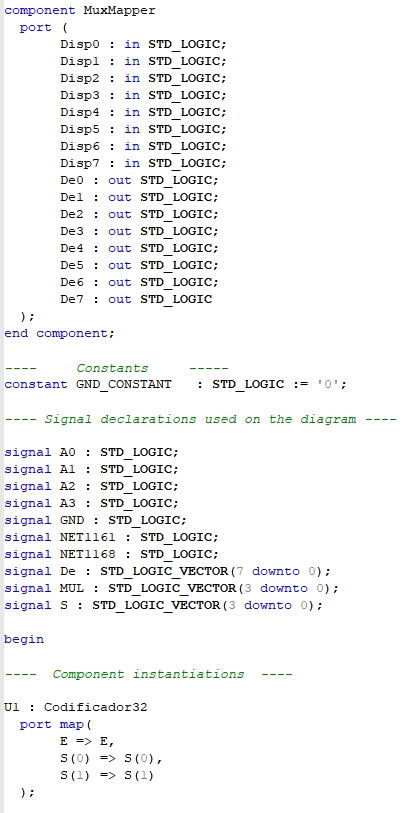
**Anexo 5.3**

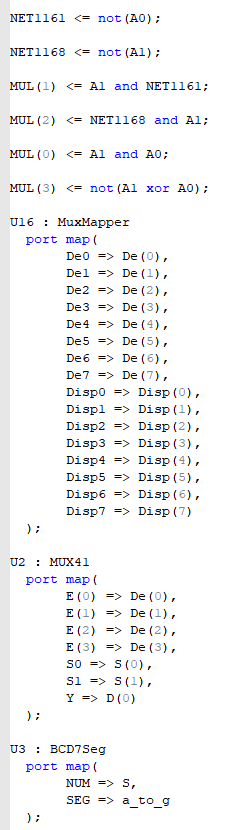
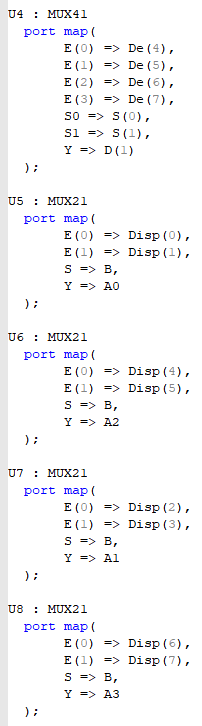
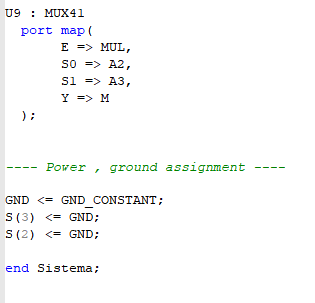
**Diseño**



**Anexo 5.4**

**Código**

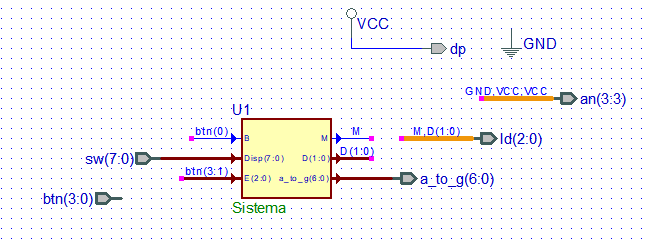




**Anexo 6: Diseño de alto nivel**

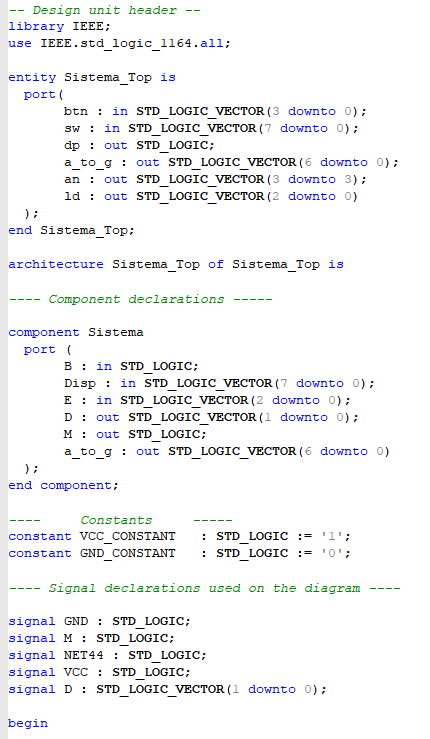
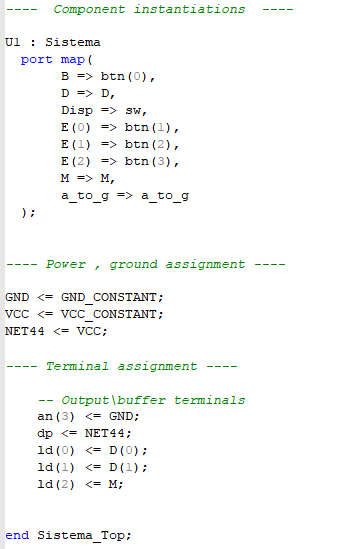
**Anexo 6.1**

**Diseño**



**Anexo 6.2**

**Código VHDL**



**Anexo 6.3**

**Tabla de resultados**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SW7** | **OFF** | **OFF** | **OFF** | **OFF** | **ON** |
| **SW6** | **OFF** | **OFF** | **OFF** | **ON** | **OFF** |
| **SW5** | **OFF** | **OFF** | **OFF** | **OFF** | **ON** |
| **SW4** | **OFF** | **OFF** | **OFF** | **OFF** | **OFF** |
| **SW3** | **OFF** | **OFF** | **OFF** | **OFF** | **ON** |
| **SW2** | **OFF** | **ON** | **ON** | **ON** | **OFF** |
| **SW1** | **OFF** | **OFF** | **OFF** | **OFF** | **ON** |
| **SW0** | **OFF** | **OFF** | **ON** | **OFF** | **OFF** |
| **BTN3** | **OFF** | **OFF** | **OFF** | **ON** | **OFF** |
| **BTN2** | **OFF** | **OFF** | **ON** | **OFF** | **OFF** |
| **BTN1** | **OFF** | **ON** | **OFF** | **OFF** | **OFF** |
| **BTN0** | **OFF** | **OFF** | **OFF** | **OFF** | **ON** |
| **LD2** | **OFF** | **OFF** | **ON** | **OFF** | **ON** |
| **LD1** | **OFF** | **OFF** | **OFF** | **OFF** | **ON** |
| **LD0** | **OFF** | **ON** | **OFF** | **ON** | **OFF** |
| **AN3** | **ON** | **ON** | **ON** | **ON** | **ON** |
| **a\_to\_g** | **0** | **1** | **2** | **3** | **0** |